[0086] With body voltage V_B applied to body electrode 116, gate-to-body bias voltage V_{GB} is applied between gate electrode 112 and body electrode 116 by applying a DC gate voltage V_G to gate electrode 112. Gate-to-body voltage V_{GB} is specifically defined as:

$$V_{GB} = V_G - V_B \tag{11}$$

where gate voltage V_G is defined relative to the same arbitrary reference point, e.g., ground, as plate voltage $\underline{V_P}$ ~~V_G~~ and body voltage V_B. Gate-to-body voltage V_{GB} is generally at least zero and is normally positive. As discussed further below, voltage V_{GB} is normally substantially constant or is controlled as a function of plate-to-body voltage V_R.

[0089] The capacitance of the gate-enhanced junction varactor of Fig. 8 is taken between plate electrode 114 and body electrode 116. When the varactor is employed in electronic circuitry having a capacitance signal path for receiving the varactor, electrodes 114 and 116 therefore lie in the capacitance path. Accordingly, body region 100 and plate region 102 are in the capacitance signal path. Gate electrode 112 is outside the capacitance signal path. Junction depletion region ~~regions~~ 118 and part or all of surface depletion region 126 variously serve as capacitive dielectric for the varactor.

[0094] Fig. 8 presents an example in which gate region 131 is divided into three gate portions 131A, 131B, and 131C. The situation in which region 131 consists of three portions 131A - 131C is also presented in the implementations/variations of Figs. ~~Fig.~~ 15 - 17, 20, and 21 (discussed further below). Region 131 can have as little as two gate portions. Figs. 12 - 14, 18, 19, 22, and 29 (also discussed further below) illustrate implementations/variations of the varactor of Fig. 8 in which region 131 is divided into two gate portions 131A and 131B.

[0110] With the foregoing in mind, the varactor of Fig. 8 operates in the following way. The relationship between plate-to-body V_R and gate-to-body voltage V_{GB} is typically controlled so that voltage V_{GB} is at an initial bias value V_{Gbi} sufficient to cause inversion layer 130 to be fully present when voltage V_R is zero. Let V_{T0max} represent the zero-point gate-to-body threshold voltage V_{T0} of the inversion portion, e.g., inversion portion 130C in the example of Fig. 8, having the highest threshold voltage V_{T0}. Gate-to-body bias value V_{Gbi} is then greater than or equal to V_{T0max}.

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[0117] The increase in plate-to-body voltage V_R is applied (with slight resistive diminishment) to inversion layer 130 by way of undepleted material 124 of plate region 102. With gate-to-body voltage V_{GB} being constant, thickness t_{ds} of surface depletion region 126 may initially remain approximately constant as voltage V_R is raised above V_{Rmin} should minimum value $\underline{V_{Rmin}}$ ~~V_{min}~~ be less than zero. If the potential that voltage V_R produces in layer 130 does not exceed the potential that voltage V_{GB} produces in layer 130 when voltage V_R is at V_{Rmin}, raising voltage V_R above V_{Rmin} causes a point to be is reached at which the electrical potential that voltage V_R produces in layer 130 exceeds the electrical potential that voltage V_{GB} produces in layer 130. This situation is present whenever voltage V_R is greater than zero. Plate-to-body voltage V_R then controls the electrical potential of layer 130 and, consequently, thickness t_{ds} of depletion region 126. Further increase in voltage V_R causes thickness t_{ds} to increase.

[0146] Components 150, 152, 154, 160, 162, 166, 164, 168, 170, 172, 174, 176, and 178 in the p-channel varactor of Fig. 10 are respectively configured the same as components 100, 102, 104, 110, 112, 114, 116, 118, 120, 122, 124, 126, and 128 in the n-channel varactor of Fig. 8. Likewise, inversion layer 180 forms at the same relative location in the varactor of Fig. 10 as does inversion layer 130 in the varactor of Fig. 8.

[0151] With three gate portions 181A - 181C being present in the example of Fig. 10, inversion layer 180 in the varactor of Fig. 10 consists specifically of three variably appearing inversion portions 180A, 180, and 180C that respectively appear/disappear along the upper surfaces of gate portions 181A - 181C. Each gate portion includes a corresponding portion of surface depletion region 176 in the varactor of Fig. 10. Hence, gate portions 181A - 181C respectively have upper surface depletion portions 176A, 176B, and 176C which together form surface depletion region 176.

[0155] The relationship derived in U.S. application 09/903,059 for transition voltage V_X provides good approximations to the values V_X of plate-to-body voltage V_R at which each of variably appearing portions of inversion layer 130 disappears here subject to the assumption that net dopant concentration N_B of the body material that forms surface depletion region 126 and body-side portion 120 of junction depletion region 118 is uniform (constant). This relationship is repeated below:

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$$V_X = V_{GB} - V_{FB} + \frac{K_{SC}\varepsilon_0 q N_B}{C_{GDA}^2} - 2\Phi_{Fp} - \sqrt{\frac{2K_{SC}\varepsilon_0(V_{GB} - V_{FB})}{C_{GDA}^2} + \left(\frac{K_{SC}\varepsilon_0 q N_B}{C_{GDA}^2}\right)^2} \quad (24)$$

where V_{FB} is the flat-band voltage, K_{SC} is the permittivity constant of the semiconductor material (typically silicon), ε_0 (again) is the permittivity of free space, q (again) is the electronic charge, C_{GDA} is the areal capacitance of gate dielectric layer 110, and Φ_{Fp} is the Fermi potential of the pertinent semiconductor material that forms surface depletion region 126.

[0165] Combining Eqs. 26 - 32 yields the following relationship for zero-point gate-to-body threshold voltage V_{T0} for a gate portion and thus for its portion of inversion layer 130 or 180:

$$V_{T0} = \pm\left(\frac{kT}{q}\right)\ln\left(\frac{N_{POLY}}{n_i}\right) \pm \left(\frac{kT}{q}\right)\ln\left(\frac{N_B}{n_i}\right) \pm \frac{2t_{GD}}{K_{GD}}\sqrt{\frac{K_{SC}N_B kT}{\varepsilon_0}\ln\left(\frac{N_B}{n_i}\right)} \quad (33)$$

where the upper signs (all pluses) apply when the pertinent semiconductor in the gate portion is of p-type conductivity, and the lower signs (all minuses) apply when the pertinent semiconductor material in the gate portion is of n-type conductivity. The pertinent semiconductor material for the first (N_{POLY}) term in Eq. 33 is the polycrystalline semiconductor material in the portion of gate electrode 112 or 162 in that gate portion. The pertinent semiconductor material for the second (N_B) and third (also N_B) terms in Eq. ~~Eqs.~~ 33 is the monocrystalline semiconductor material in the surface depletion portion of that gate portion. Examination of Eq. 33 indicates that threshold voltage V_{T0} for a gate portion can be adjusted by adjusting its gate dielectric thickness t_{GD}, net dopant concentration N_B in the surface depletion portion of that gate portion, the conductivity types of the polycrystalline semiconductor material in the portion of gate electrode 112 or 162 in that gate portion, and net dopant concentration N_{POLY} of the polycrystalline semiconductor material in the portion of electrode 112 or 162 in that gate portion.

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[0167] Similar comments apply to transition ~~threshold~~ values V_X of plate-to-body voltage V_R. Any statement that a portion of inversion layer 130 or 180 disappears (or appears) when

voltage V_R is at one of the corresponding V_X values at a given value of gate-to-body voltage V_{GB} is to be interpreted as meaning that the inversion portion largely disappears (or appears) at that V_X value, i.e., the inversion portion disappears (or appears) over a short V_R range which includes that V_X value. This phenomena is illustrated in Figs. 24, 28, and 31 (discussed further below) which show how the varactor (lineal) capacitance in implementations of the present varactor undergoes a sharp change in value as voltage V_R passes through a short range that includes each transition value V_X at constant gate-to-body voltage V_{GB}.

[0168] Figs. 12 - 21 illustrate implementations, or variations, of the n-channel varactor of Fig. 8 in which portions of gate region 131 are provided with different zero-point gate-to-body threshold voltages V_{T0} in accordance with the invention by (a) variously dividing gate dielectric layer 110 into multiple portions of different thicknesses, (b) providing portions of surface depletion region 126 with different values of average net dopant concentration N_B, or/and (c) constituting gate electrode <u>112</u> ~~12~~ as upper metallic layer 112U and lower layer 112L consisting of doped polycrystalline semiconductor material divided laterally into portions of both (n-type and p-type) conductivity types. Alternatively or additionally, polycrystalline semiconductor material of one conductivity type in lower gate electrode layer 112L can be laterally divided into multiple portions having different values of average net dopant concentration N_{POLY}.

[0181] Dopant concentration N_{BB} of surface depletion portion 126B is greater than dopant concentration N_{BA} of surface depletion portion 126A in the varactor of Fig. 13. Per Eq. 33, zero-point gate-to-body threshold voltage V_{T0} increases as dopant concentration N_B increases in the n-channel case where the semiconductor material of surface depletion region 126 is p-type. Inasmuch as gate region 131B is of greater threshold voltage V_{T0} than gate portion 131A, gate portions 131A and 131B progressively increase in threshold voltage V_{T0} as depletion portions 126A and 126B of respective gate portions 131A and 131B progressively increase in dopant concentration N_B. Consequently, portions 130A and 130B <u>of</u> ~~or~~ inversion layer 130 appear/disappear at progressively increasing values of threshold voltage V_{T0} as depletion portions 126A and 126B respectively associated with inversion portions 130A and 130B progressively increase in dopant concentration N_B.

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[0182] The preceding threshold-voltage/dopant-concentration relationship extends, as indicated below in connection with the n-channel varactor of Fig. 17, to implementations of the present n-channel varactor in which gate region 131 is divided into three or more portions, each having a surface depletion portion of different average dopant concentration N_B than the other surface depletion portions. Subject to the voltage polarities being reversed, this relationship also applies to implementations of the present p-channel varactor in which gate region 181 ~~131~~ is divided into two or more portions, each having a surface inversion portion of different dopant concentration N_B than the other surface depletion portions. Accordingly, the portions of gate region 131 or 181 progressively increase in the magnitude of threshold voltage V_{T0} as the portions of surface depletion region 126 or 176 progressively increase in dopant concentration N_B, and vice versa. Likewise, the portions of inversion layer 130 or 180 appear/disappear at progressively increasing V_{T0} magnitude as the surface depletion portions respectively associated with the inversion portions progressively increase in concentration N_B, and vice versa.

[0183] Surface depletion portion 126A meets plate region 102 in the varactor of Fig. 13. Since surface depletion portion 126B is of greater dopant concentration N_B than depletion portion 126A, depletion portion 126B is continuous with a surface depletion portion more lightly doped than portion 126B. This relationship involving depletion portions 126A and 126B can be extended to situations in which surface depletion region 126 or 176 is divided into more than two portions having different N_B values. For the general situation in which the surface depletion portions have the threshold-voltage/dopant-concentration ~~threshold-voltage/ dopant-concentration~~ relationship described in the previous paragraph, each surface depletion portion meets plate region 102 or 152 or/and is continuous with another surface depletion portion more lightly doped than that surface depletion portion.

[0194] Rather than being of opposite conductivity types, gate electrode portions 112LA and 112LB can be of the same conductivity type, either p-type or n-type, but at different values of gate electrode dopant concentration N_{POLY} in a variation of the varactor of Fig. 14. If electrode portions 112LA and 112LB are both n-type and thus of opposite conductivity type to body region 100, electrode portion 112LA is doped more heavily ~~lightly~~ n-type than is electrode portion 112LB. In accordance with Eq. 33, gate portion 131B meets the requirement of having a higher value of zero-point gate-to-body threshold voltage V_{T0} than

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gate portion 131A. The reverse dopant-concentration relationship arises if electrode portions 112LA and 112LB are both p-type and thus of the same conductivity type as body region 100. Per Eq. 33, electrode portion 112LA is doped more lightly ~~heavily~~ p-type than is electrode portion 112LB. Since p-n junction 190 is absent in this variation, upper metallic gate electrode layer 112U can be deleted.

[0196] Consider the situation for the preceding variations of the n-channel varactor of Fig. 8 in which gate portion 131A separates gate portion 131B from plate region 102. With portions 112LA and 112LB of gate electrode layer 112L both being of n-type conductivity and thus of opposite conductivity type to body region 100, electrode portion 112LA which is more heavily ~~lightly~~ doped than electrode portion 112LB extends between electrode portion 112LB and a location above plate region 102 such that electrode portion 112LB is spaced laterally apart from region 102. The same occurs when electrode portions 112LA and 112LB are both of p-type conductivity and thus of the same conductivity type as body region 100 except that electrode portion 112LA is now more lightly ~~heavily~~ doped than electrode portion 112LB.

[0217] In a semiconductor fabrication process ~~process,~~ that includes a capability for providing insulated-FETs with threshold-adjust ion implantations, the threshold-adjust capability can be utilized to provide the portions of surface depletion region 126 or 176 with different values of net dopant concentration N_B in manufacturing a varactor such as that of Fig. 13 or 17. If a process for manufacturing complementary insulated-gate FETs includes a capability for manufacturing gate electrodes of both n-type conductivity and p-type conductivity, this capability can be employed to provide gate electrode 112 (112L) or 162 (162L) with portions of opposite conductivity type in fabricating a varactor such as that of Fig. 14.

[0225] Lineal capacitance C_{VW} was determined as a function of plate-to-body bias voltage V_R for the simulated varactor of Fig. 22, 26, or 29 by replacing DC bias voltage V_R with a frequency-dependent plate-to-body voltage $\underline{v_R}$ ~~V_R~~ consisting of bias voltage $\underline{V_R}$ ~~v_R~~ and a small-signal AC variation v_r at frequencies, primarily 10 MHz, in the high-frequency regime while gate-to-body voltage V_{GB} was held at fixed initial value V_{Gbi}. Body voltage V_B was held at zero so that the v_r small-signal frequency was applied specifically to plate region

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102. Initial value V_{Gbi} was sufficiently great to cause inversion layer 130 to be fully present at bias voltage V_R equal to zero.

[0226] The frequency of the v_r small signal was also varied across a range extending from 1 Hz to 1 ~~Hz-to-1~~ GHz. No significant difference in the C_{VW} dependence on the frequency of the v_r small signal occurred across the 1Hz-to-1GHz high-frequency range. In this regard, the capacitive behavior of the present gate-enhanced junction varactor is determined by the variation of the electrical charges in junction depletion region 118 and surface depletion region 126 and therefore by a majority charge-carrier effect. Consequently, constancy of the capacitive behavior across the high-frequency regime is theoretically expected.

[0243] Capacitance C_{VW} for each of the four right-most curves in Fig. 28 dropped more sharply with increasing plate-to-body voltage V_R as voltage V_R passed through each of transition values V_{XD}, V_{XC}, V_{XB}, and V_{XA} than at a location midway between each consecutive pair of transition values V_{XA} - V_{XD}. However, the C_{VW} drop in passing through each of transition values V_{XA} - V_{XD} for each of these four curses was considerably more gradual than the C_{VW} drop that occurred in passing through transition values V_{XA} and V_{XB} for each of the four curves in Fig. 24. Hence, capacitance C_{VW} varied more gradually with voltage V_R in the four-transition-voltage varactor of Fig. 26 than in the <u>two-transition-voltage</u> ~~two-transition-voltage~~ varactor of Fig. 22. Increasing the number of gate portions in gate region 131 typically leads to a more gradual C_{VW} variation with voltage V_R at constant gate-to-body voltage V_{GB}.

[0268] More particularly, again consider the situation in which body voltage V_B varies between V_{LL} and V_{HH} - V_{Gbi}. Again assume that electronic circuit 230 does not significantly affect DC plate voltage V_P. In the presence of shifter 234, the fixed value of plate voltage V_P is then substantially V_{HH} - V_{LS}. Hence, plate-to-body voltage V_R varies across a minimum-to-maximum range extending from V_{Gbi} - V_{LS} to V_{HH} - V_{LL} - V_{LS} when shifter 234 is present. The length of the V_{Rmin}-to-V_{Rmax} range is V_{HH} - V_{LL} - <u>V_{Gbi},</u> ~~V_{LS},~~ the same as arises when shifter 234 is absent.

[0272] The general circuitry of Fig. 32 can be readily modified to use a p-channel version of the present gate-enhanced junction varactor in place of n-channel junction varactor C1.

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One way of implementing this modification is to reconfigure the circuitry so that it is interconnected in a complementary (mirror-image) manner to what is shown in Fig. 32. That is, high-bias capacitance signal path line 236 can be connected directly to voltage sources 244 and 246 in control system 232. Using the electrode reference symbols of Fig. 11, low-bias capacitance signal path line 238 is connected to plate electrode 164 of the p-channel varactor. With the polarity direction of voltage sources 244 and 246 reversed, gate ~~plate~~ electrode 162 and body electrode 166 of the p-channel varactor are respectively connected to voltage sources 244 and 246. Due to the polarity direction reversal, voltage source 244 provides gate voltage V_G at a lower value than body voltage V_B provided by voltage source 246. When present, level shifter 234 is connected between circuit 230 and the V_{LL} supply.

[0279] Varactor control system 232 in the circuitry of Fig. 33 is configured with respect to, and controls, varactor C1 in the same manner as in the circuitry of Fig. 32. Control system 232 in the circuitry of Fig. 33 is also configured with respect to, and controls, varactor C2 the same as varactor C1. Hence, system 232 furnishes each of varactors C1 and C2 with gate voltage V_G and body voltage V_B at values which normally vary during circuitry operation but whose difference V_{GB} is held largely constant at initial value V_{GBi}. In particular, high-bias DC voltage source 244 provides gate voltage V_G on high-bias control line 240 to gate electrode 112 of each of varactors C1 and C2. Low-bias voltage source 246 provides body voltage V_B on low-bias control line 242 ~~248~~ to body electrode 116 of each of varactors C1 and C2.

[0280] Neither low-bias capacitance signal path line 238 ~~236~~ nor one or more low-bias impedance components analogous to low-bias impedance ZL in the circuitry of Fig. 32 appears in the circuitry of Fig. 33. Rather than being connected through electrical lines 248 and 250 to low-bias path line 238, voltage sources 244 and 246 in control system 232 are connected by electrical lines 248 and 250 directly to the V_{LL} low voltage supply in the circuitry of Fig. 33.

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[0312] Fig. 37 illustrates a layout, in accordance with the invention, of an implementation of the n-channel junction varactor of Fig. 8, specifically an embodiment of the implementation of Fig. 14. ~~19.~~ Fig. 38 depicts a cross section of the n-channel varactor of Fig. 37 taken along a vertical plane extending through plate region 102. The varactor of Figs. 37 and 38 contains components 132, 134, 136, 138, 140, 142, and 144 as generally

described above in connection with the n-channel junction varactor implementation of Fig. 9b. Lower gate electrode layer 112L here consists of n++ polysilicon portion 112LA and p++ polysilicon portion 112LB.

[0317] The present n-channel junction varactor, such as that of Figs. 37 and 38, ~~38~~ is fabricated according to a suitable manufacturing process, typically one having a capability for providing n-channel insulated-gate FETs and thus invariably also p-n diodes, in accordance with the selected layout. The fabrication operation can, for example, be performed according to the semiconductor manufacturing process described in Bulucea et al, U.S. patent application 09/540,442, filed 32 March 2000, now U.S. Patent 6,548,842 B1, the contents of which are incorporated by reference herein.

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